WHAT IS CLAIMED IS:

1. A digital phase-locked loop compiler, comprising:

a phase digital converter for comparing a feedback signal at an output frequency and a reference signal at a reference frequency, sampling the compared result at a predetermined frequency, and outputting a digital phase adjusting signal;

a digital-to-analog voltage converter for converting the digital phase adjusting signal into an analog phase adjusting signal;

a voltage-control oscillator for outputting an output signal at the output frequency under the adjustment of the analog phase adjusting signal; and

a post-divider for feeding back and dividing down the output signal to the phase digital converter based upon a predetermined post adjusting value.

2. The compiler in claim 1 further comprises a pre-divider for dividing down the input signal into the reference signal at the reference frequency based upon a pre-adjusting value.

3.The compiler in claim 1 further comprises a high-frequency oscillator for issuing a sampling signal at a sampling frequency to sample the feedback signal at the output frequency and the reference signal at the reference frequency .

4. The compiler in claim 1 further comprises an out-divider for dividing down the output signal at the output frequency to produce a desired output signal at a desired output frequency according to an output adjusting value.

5. The compiler in claim 1, wherein the phase digital converter further comprises a phase-frequency detector for outputting a value-modifying signal according to the feedback signal at the output frequency and the reference signal at the reference frequency.

6. The compiler in claim 1, wherein the phase digital converter further comprises an up-down converter for outputting an adjusting signal according to the value-modifying signal.

7. The compiler in claim 1, wherein the phase digital converter further comprises an arithmetic logic unit for outputting the phase adjusting value according to the adjusting signal.

8. The compiler of claim 1 further comprises a built-in self-tester.

9. The compiler in claim 1, wherein the predetermined post adjusting value for the post divider is adjustable.

10. The compiler of claim 1, wherein the sampling frequency is 360 times the comparable input frequency.

11. The compiler of claim 1, wherein the feedback frequency has a preset value.

12. The compiler of claim 1, wherein the pre adjusting value is automatically set by the digital phase-locked loop compiler according to the input frequency.

13. The compiler of claim 1, wherein the post adjusting value is set according to the required output frequency.

14. The compiler of claim 1, wherein the output adjusting value is set according to the required output frequency.

15. The compiler of claim 1, wherein the phase adjusting value is a 9-bit digital signal.